REMARKS

Present Status of the Application

The Office Action rejected claims 1-9 under 35 U.S.C. 103(a), as being unpatentable over Shimoda; Kenji et al. (U.S. 5404248) in view of Lahmeyer; Charles R (U.S. 4649541 A). The Office Action also rejected claims 1-9 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 5-10 of U.S. Patent No. US 6662335 B1 in view of Roth; Ron M. et al. (U.S. 5719884 A). Applicants have amended a drawing and specification. Applicants have also agreed to sign the terminal disclaimer to overcome double patenting. After entry of the foregoing amendments, claims 1-6 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

The Office Action rejected claims 1-9 under 35 U.S.C. 103(a), as being unpatentable over Shimoda; Kenji et al. (U.S. 5404248, "Shimoda" hereinafter) in view of Lahmeyer; Charles R (U.S. 4649541 A, "Lahmeyer" hereinafter). Applicants respectfully traverse the rejections for at least the reasons set forth below.

It is asserted that the disclosure of the Shimoda in view of the "RAM and One of Three Selectors 30" in the Lahmeyer can render claim 1 obvious. More particularly, it is asserted that "the internal buffer RAM 30 in Figure 1 of Lahmeyer is only used for the error correction processing of Reed-Solomon Codes internal to the Reed-Solomon decoder, hence Lahmeyer

teaches storing the error detection codes into a second internal buffer RAM30 in Figure 1 of the Lahmeyer other than the external memory 257 in Figure 9B of the Shimoda." However, the "RAM and One of Three Selectors 30" of FIG 1in the Lahmeyer can not remedy the deficiency of the Shimoda reference.

Lahmeyer relates to a "Reed-Solomon decoder" with dedicated hardware for five sequential algorithms is provided with **overall pipelining by memory swapping** between input, processing and output memories, and internal pipelining through the five algorithms. (Abstract) As described in the Col. 5, Lines 11-14 of the Lahmeyer, "The use of a RAM interface with the input and output modules eliminates data transfer delays by keeping data in place in memory while switching access to modules 42 and 48 as needed." The RAM 30 is used for keeping data while switching access to modules 42 and 48, to achieve the overall pipelining by memory swapping. In addition, as described in the Col. 5, Lines 26-28 of the Lahmeyer, for pipelining consideration, "the RAM memory 30 is accessed by two modules in the decoding means 40 during decoding...."

Shimoda and Lahmeyer, either implicitly or explicitly, do not disclose, teach, or suggest the feature of "a second decoder, for reading the error detection codes from the memory, storing the error detection codes into a second buffer other than the memory, and performing a second decoding on the data stored in the memory when the data stored in the memory is sufficient to be assembled as a complete data block; **and a host interface, for inspecting whether the error detection codes in the second buffer are correct or not, if correct, the data stored in the memory will be output to a host**" as claimed in the amended claim 1. The amendments

addressed to claim 1 can be supported by the disclosure in the paragraph which begins at line 6, page 8, of the specification, which states "After the RSPC decoder 426 decodes decoding all the outer-code parity, the host interface 428 inspects whether the error detection codes in the error detection code file 422 corresponding to the 16 data sectors are correct. If the error detection codes are correct, the data stored in the memory 421 is sent to the host 430."

Even if combined, Shimoda and Lahmeyer do not achieve the claimed invention in amended claim 1 because the RAM memory 30 of the teaching of the Lahmeyer is accessed by two modules during decoding and keeps data in place in memory while switching access to these two modules. There is no teaching or suggestion that "inspecting whether the error detection codes in the second buffer are correct or not, if the error detection codes are correct, the data stored in the memory will be output to a host."

For at least the foregoing reasons, Applicant respectfully submits that independent claim 1 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-6 patently define over the prior art as well.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-6 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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